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(74) Agents: GAGNEBIN, Charles, L., III et al.; Weingarten, Schurgin, Gagnebin & Hayes LLP, Ten Post Office Square, Boston, MA 02109 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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(54) Title: INTEGRATED PACKAGING OF MICROMECHANICAL SENSORS AND ASSOCIATED CONTROL CIRCUITS

(57) Abstract: A micromechanical sensor is fabricated on a semiconductor wafer, and a control circuit is fabricated on another semiconductor wafer. A cavity is etched on the back side of the control circuit wafer, the cavity being formed such that the sensor on the other wafer fits within the cavity when the wafers are brought together in an adjoining relationship. Through-holes are etched through the back side of the control circuit wafer to allow access to electrical contact points, and a patterned layer of metal is deposited to form electrical interconnections between the electrical contact points and termination points on the back side of the wafer via the through-holes. The termination points are arranged such that electrical contacts of the sensor contact the termination points when the wafers are placed in the adjoining relationship. The wafers are then cleaned and bonded together in the adjoining relationship. In a typical process the wafers contain multiple sensors and control circuits, respectively, and thus the bonded wafers are diced to yield individual bonded sensor-circuit pairs. The bonded pairs are then packaged in an integrated-circuit package such as a leadless chip carrier in a known manner.

TITLE OF THE INVENTION

INTEGRATED PACKAGING OF MICROMECHANICAL SENSORS AND ASSOCIATED CONTROL CIRCUITS

CROSS REFERENCE TO RELATED APPLICATIONS

--None--

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

--Not Applicable--

BACKGROUND OF THE INVENTION

The present invention is related to the field of sensors and their associated sensor control circuitry, and more particularly to the mechanical packaging of systems such as gyroscopes and accelerometers that employ sensors and sensor control circuitry.

Many types of systems use sensors to detect the value of a property of a physical system and to generate a corresponding electrical signal representative of the sensed value. The electrical signals from sensors are commonly provided to electrical circuitry off chip or in adjacent locations on chip in order to enable a desired function to be performed. For example, inertial guidance systems use gyroscopes and accelerometers to monitor the orientation of an object in flight and the direction and magnitude of forces experienced by the object. The gyroscopes and accelerometers rely on electromechanical sensors that translate particular types of motion, such as rotational or linear acceleration, into corresponding electrical signals.

It has become possible to fabricate very small or micromechanical sensors out of silicon wafers of the type used in the manufacture of integrated circuits.

Micromechanical sensors are comparable in size to integrated circuits (IC's). During fabrication of micromechanical sensors, silicon wafers containing numerous sensors are diced into individual sensors, and the sensors are individually mounted into packages of the type used for integrated circuits, such as sealed leadless ceramic chip carriers. The packaged sensor is then mounted on a printed circuit board along with an associated control circuit, usually an IC itself and packaged in a similar manner. The sensor and control circuit, along with other circuit components as required, collectively perform the desired sensing function.

One of the drawbacks of the above-described method of packaging sensor-based systems is that individual unprotected sensors must be handled during packaging operations, potentially reducing yield and increasing manufacturing costs. Also, the sensor package is generally significantly larger and more expensive than the sensor, so the package contributes notably to the dimensions and cost of the assembled printed circuit board. Also, mounting the sensor in a package such as a chip carrier limits how close the sensor can be placed to the control integrated circuit, which in turn can unnecessarily limit the electrical performance of the sensor-based system or increase the susceptibility to noise.

It would be desirable to improve the cost, size, and performance of systems employing micromechanical sensors and associated control circuitry.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, a method of fabricating and packaging micromechanical sensors and their associated control circuitry is disclosed that eliminates the need for a separate carrier package for the sensor. The disclosed packaging method advantageously eliminates the handling of exposed sensors during packaging operations, and results in closer placement of the sensor and its associated control circuit, so that costs are reduced and greater system performance can be achieved.

In the disclosed fabrication method, a micromechanical sensor is fabricated on a semiconductor wafer, and a control circuit is fabricated on another semiconductor wafer. A cavity is etched on the back side of the control circuit wafer, the cavity being formed such that the raised portion of a sensor fabricated on the other wafer fits within the cavity when the wafers are brought together in an adjoining relationship. Through-holes are etched through the back side of the control circuit wafer to allow access to electrical contact points of the sensor circuit, and a patterned layer of metal is deposited to form electrical interconnections between the electrical contact points and termination points on the back side of the control circuit wafer via the through-holes. The termination points are arranged such that electrical contacts of the sensor contact the termination points when the wafers are placed in the adjoining relationship. The wafers are then cleaned and bonded together in the adjoining relationship. In a typical process the respective wafers contain multiple sensors and control circuits, respectively, and thus the bonded wafers are diced to yield individual bonded sensor-circuit pairs. The bonded pairs are then packaged in a known manner.

The fabrication method eliminates the need for

separate packages for the sensor and control circuit. Also, processing is done at the wafer clean room level so that the handling of individual exposed sensors is eliminated. The sensor and control circuit in each bonded pair are placed in intimate contact, thus reducing overall size and improving electrical performance, and the pairs can be packaged using conventional integrated-circuit packaging technology.

Other aspects, features, and advantages of the present invention are disclosed in the detailed description which follows.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

Figure 1 is a flow diagram of a sensor packaging method according to the present invention;

Figures 2 through 5 are schematic depictions of a control-circuit wafer at various stages in the packaging method of Figure 1; and

Figure 6 is a schematic depiction of a bonded sensor and control circuit pair resulting from the packaging method of Figure 1.

DETAILED DESCRIPTION OF THE INVENTION

In the process of Figure 1, an array of control circuits are fabricated on a semiconductor wafer at step 10 using conventional integrated-circuit fabrication techniques. The resulting control circuits may be completely custom-designed, or may be of the type known as "application-specific integrated circuits" or ASICs. The layout of the array of control circuits mirrors that of a corresponding array of sensors on a separate wafer, so that when the wafers are placed in an aligned adjoining relationship each control circuit is aligned with a corresponding sensor. This arrangement facilitates a subsequent fabrication step in which the wafers are bonded together, as described below.

Figure 2 shows a site on a wafer 30 where a single control circuit 32 is formed. Figures 2 through 6 show the results of steps from the process of Figure 1 at the site for a single sensor and control circuit pair. However, it is to be understood that the same results are obtained for each sensor and control circuit pair from the two wafers being processed, so that a complete picture of the process results would simply show an array of identical sites on the wafers.

In step 12 of Figure 1, the upper portions of the control circuit wafer 30 are removed by known mechanical and/or chemical means, resulting in a thinned wafer 30 as shown in Figure 3

In step 14, through-hole vias 34 are etched in the backside of the control circuit wafer 30 to allow access to sensor interconnection points or metallizations 33 from the backside of the control circuit wafer 30. In step 16, a second etch process is conducted to form cavities 36 for the sensors on the backside of the control circuit wafer. The results of these etching steps are shown in Figure 4.

In step 18, the back side of the control circuit wafer 30 is metallized with a patterned layer 38 of metal to create electrical interconnections in the previously-etched vias to electrical input and output points of the control circuit. The interconnections extend to include contact pads on the back side of the control circuit wafer as a part of layer 38. Corresponding contact points 39 on the sensors for input and/or output signals (I/O) are pressed against the contact pads during subsequent bonding of the wafers to complete the electrical interconnection between them. The result of the metallization step 18 is shown in Figure 5.

In step 20, the control circuit wafer 30 and a sensor wafer 40 are cleaned under high vacuum conditions. While this high vacuum is maintained, the wafers are

bonded together in step 22 using heat and/or pressure in known bonding techniques. The result of the bonding is a bonded component as shown in Figure 6 including a control circuit 32 and an associated sensor 42 interconnected with the control circuit via pads in layers 38 that contact the sensor contacts 39 and disposed in the etched cavity 36 on the back side thereof.

In the remaining steps 24 and 26, the bonded wafers are diced and the individual bonded components are packaged in an integrated circuit package such as a leadless chip carrier. The packaged component can then be mounted on a printed circuit board or other circuit substrate that provides power inputs and receives instrument outputs as required by the system in which it is used.

While the above description is of a preferred embodiment and best mode, the sensor circuit and control circuit can be placed both on outer wafer surfaces, or the control circuit placed in a back side cavity of the sensor wafer.

A method of fabricating and packaging micromechanical sensors and their associated control circuits has been shown. It will be apparent to those skilled in the art that modification to and variation of the above-described methods and apparatus are possible without departing from the inventive concepts disclosed herein. Accordingly, the invention should be viewed as limited solely by the scope and spirit of the appended claims.

CLAIMS

What is claimed is:

1. A method of packaging a micromechanical sensor with an associated control circuit, comprising:

fabricating the sensor on a front side of a first wafer of semiconductor material, said sensor having electrical contact points of electrical I/O;

fabricating the control circuit on a front side of a second wafer of semiconductor material, said control circuit having electrical contacts;

forming a cavity on the back side of the second wafer, the cavity being formed such that the sensor fits within the cavity when the front side of the first wafer is placed in an adjoining relationship with the back side of the second wafer;

forming through-holes in the second wafer at locations adjacent to the cavity allowing access to the electrical contacts of the control circuit from the back side of the second wafer;

depositing a patterned layer of metal on the back side of the second wafer to form electrical interconnections to the electrical contacts of the control circuit via the through-holes, the interconnections terminating in back-side termination points arranged such that electrical contact points of the sensor contact the termination points when the wafers are placed in an adjoining relationship; and

bonding the first wafer and the metallized second wafer together in the adjoining relationship.

2. A method according to claim 1, further comprising the step of removing substrate material from the back side of the second wafer to reduce the thickness thereof.

3. A method according to claim 1, further comprising the step of cleaning the wafers prior to the bonding step.

4. A method according to claim 1, wherein the bonding step results in the wafers being bonded at least in an area adjacent to the sensor and control circuit, and further comprising the step of separating the bonded control circuit and sensor from the remainder of the bonded wafers.

5. A method according to claim 4, further comprising the step of packaging the bonded control circuit and sensor in an integrated-circuit package.

6. A method according to claim 5, wherein the integrated-circuit package is a leadless chip carrier.

7. A method according to claim 1, wherein the step of forming the cavity comprises etching the cavity.

8. A method according to claim 1, wherein the step of forming the through-holes comprises etching the through-holes.

9. A method of packaging micromechanical sensors and associated control circuits, comprising:

fabricating the sensors on a front side of a first wafer of semiconductor material;

fabricating the control circuits on a front side of a second wafer of semiconductor material, the control circuits being arranged such that each control circuit is mutually aligned with an associated sensor when the front side of the first wafer is placed in an adjoining relationship with the back side of the second wafer;

forming cavities on the back side of the second wafer, the cavities being arranged such that each sensor

on the first wafer fits within an associated cavity when the first and second wafers are placed in the adjoining relationship;

forming through-holes in the second wafer at locations adjacent to the cavities allowing access to electrical contact points on the front side of the second wafer from the back side thereof;

depositing a patterned layer of metal on the back side of the second wafer to form electrical interconnections between termination points on the back side of the wafer and the electrical contact points on the front side of the wafer via the through-holes, the termination points being arranged such that the electrical contacts on the front side of the first wafer contact the termination points when the wafers are placed in the adjoining relationship;

bonding the first and second wafers together in the adjoining relationship, the wafers being bonded together at least at points adjacent to the control circuits and sensors; and

cutting the bonded wafers into sections each including a control circuit and the associated sensor bonded thereto.

10. A method according to claim 9, further comprising the step of removing substrate material from the back side of the second wafer to reduce the thickness thereof.

11. A method according to claim 9, further comprising the step of cleaning the wafers prior to the bonding step.

12. A method according to claim 9, further comprising the step of packaging each bonded control circuit and sensor in a corresponding integrated-circuit package.

13. A method according to claim 12, wherein the integrated-circuit package is a leadless chip carrier.

14. A method according to claim 9, wherein the step of forming the cavities comprises etching the cavities.

15. A method according to claim 9, wherein the step of forming the through-holes comprises etching the through-holes.

16. A sensor and control circuit assembly, comprising:

a planar monolithic circuit substrate having a control circuit formed on a front side being generally aligned with the control circuit; and

a planar sensor substrate bonded to the circuit substrate, the sensor substrate having a micromechanical sensor formed thereon, the sensor being electrically connected to the control circuit via contact pads on the sensor substrate contacting the contact pads on the circuit substrate;

one said substrate having electrical interconnections between electrical connection points of one of the control circuit and sensor and contact pads on a backside of the one said substrate.

17. The assembly of claim 16 wherein a cavity if formed in a surface of one said substrate to accommodate one of said sensor and circuit.

18. The assembly of claim 17 wherein said cavity is in a back side of said circuit substrate.

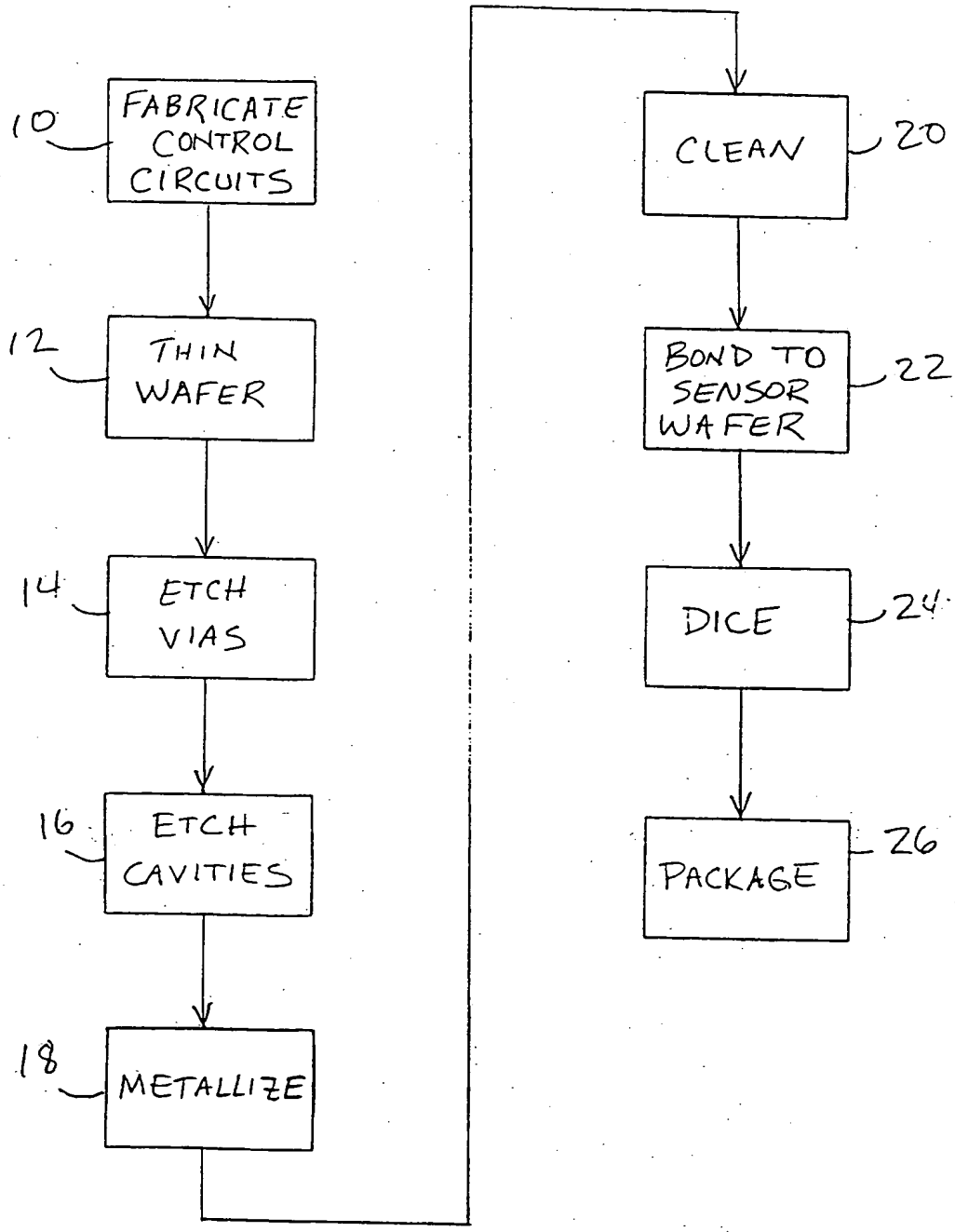

Fig. 1

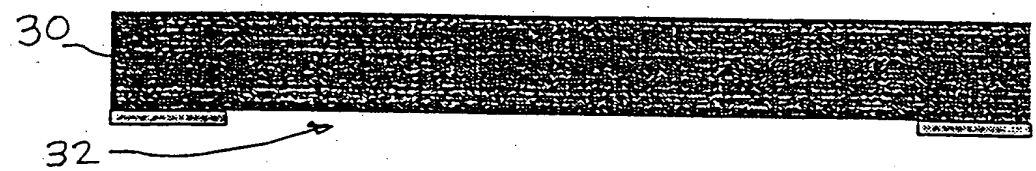

Fig. 2

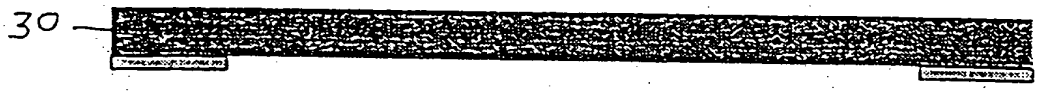

Fig. 3

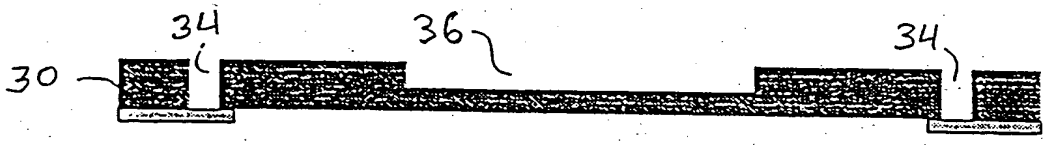

Fig. 4

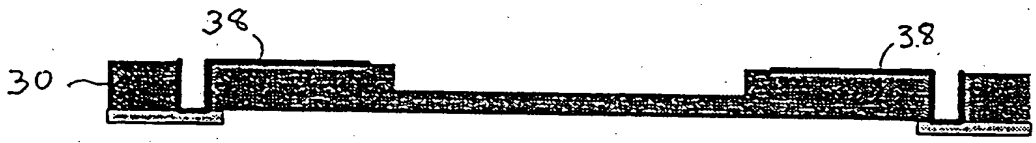

Fig. 5

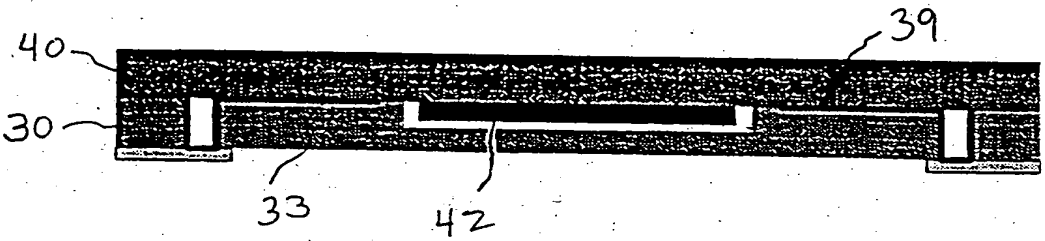

Fig. 6

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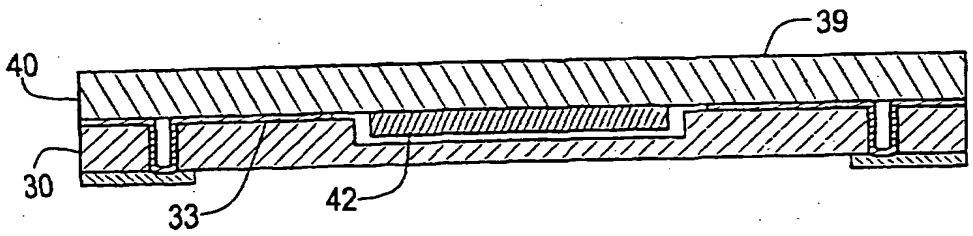
(54) Title: INTEGRATED PACKAGING OF MICROMECHANICAL SENSORS AND CONTROL CIRCUITS



(57) Abstract: A micromechanical sensor (42) is fabricated on a first semiconductor wafer (40), and a control circuit is fabricated on a front side of a second wafer (30). A cavity (36) is formed on the backside of the second wafer, the cavity is being formed such that the sensor on the wafer fits within the cavity when the wafers are brought together in an adjoining relationship. Through-holes (34) are etched through the backside of the second wafer to allow access to electrical points and a patterned layer (38) is deposited to form electrical interconnections between electrical contact points and terminal points on the backside of the wafer via through-holes. The two wafers are cleaned and bonded together. The bonded wafers are diced to yield individual bonded sensor-control circuit pairs.

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A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/48, 50, 51, 52-53, 106, 107, 110, 113, 455, 456, 458-462, 700-702, 719, 753, 977; 257/414, 417, 419; 73/861.47

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WEST, JPO, EPO, CA, INSPEC, NPL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,837,562 A (CHO) 17 November 1998 (17.11.1998), fig.5 and col-4-5.	1-18
Y, P	US 6,114,221 A (TONTI et al.) 05 September 2000 (05.09.2000), figs. 15-16, col. 3, lines 5-60.	1-18
Y	US 5,866,469 A (HAYS) 02 February 1999 (02.02.1999), fig.3B col. 3-col.4.	1-18
Y	US 5,492,596 A (CHO) 20 February 1996 (20.02.1996), see 3A-4B and col.3-col. 4.	1-18
Y	US 5,646,072 A (MAUDIE et al.) 08 July 1997 (08.07.1997), fig. 4 and col. 2, lines 59- col. 3, lines 62).	1-18

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y ----- X	US 5,721,162 A (SCHUBERT et al.) 24 February 1998 (24.02.1998), detailed description.	1-15 -------- 16-18
Y ----- X	US 5,895,233 A (HIGASHI et al.) 20 Aptil 1999 (20.04.1999), detailed description.	1-15 -------- 16-18
Y, P	US 6,143,583 A (HAYS) 07 November 2000 (07.11.2000), see detailed descrption.	1-18
Y, P	US 6,074,891 A (STALLER) 13 June 2000 (13.06.2000), detailed description.	1-18
Y	US 5,712,162 A (SCHUBERT et al.) 24 February 1998 (24.02.1998), see entire document.	1-18

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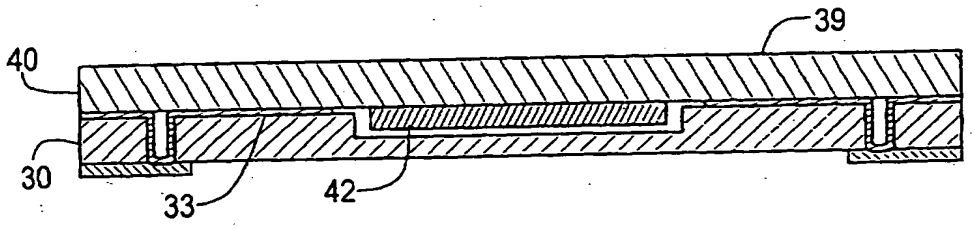
(54) Title: INTEGRATED PACKAGING OF MICROMECHANICAL SENSORS AND CONTROL CIRCUITS



(57) Abstract: A micromechanical sensor (42) is fabricated on a first semiconductor wafer (40), and a control circuit is fabricated on a front side of a second wafer (30). A cavity (36) is formed on the backside of the second wafer, the cavity is being formed such that the sensor on the wafer fits within the cavity when the wafers are brought together in an adjoining relationship. Through-holes (34) are etched through the backside of the second wafer to allow access to electrical points and a patterned layer (38) is deposited to form electrical interconnections between electrical contact points and terminal points on the backside of the wafer via through-holes. The two wafers are cleaned and bonded together. The bonded wafers are diced to yield individual bonded sensor-control circuit pairs.

WO 01/029529 A3

TITLE OF THE INVENTION

INTEGRATED PACKAGING OF MICROMECHANICAL SENSORS AND CONTOL CIRCUITS

CROSS REFERENCE TO RELATED APPLICATIONS

--None--

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

--Not Applicable--

BACKGROUND OF THE INVENTION

The present invention is related to the field of sensors and their associated sensor control circuitry, and more particularly to the mechanical packaging of systems such as gyroscopes and accelerometers that employ sensors and sensor control circuitry.

Many types of systems use sensors to detect the value of a property of a physical system and to generate a corresponding electrical signal representative of the sensed value. The electrical signals from sensors are commonly provided to electrical circuitry off chip or in adjacent locations on chip in order to enable a desired function to be performed. For example, inertial guidance systems use gyroscopes and accelerometers to monitor the orientation of an object in flight and the direction and magnitude of forces experienced by the object. The gyroscopes and accelerometers rely on electromechanical sensors that translate particular types of motion, such as rotational or linear acceleration, into corresponding electrical signals.

It has become possible to fabricate very small or micromechanical sensors out of silicon wafers of the type used in the manufacture of integrated circuits.

Micromechanical sensors are comparable in size to integrated circuits (IC's). During fabrication of micromechanical sensors, silicon wafers containing numerous sensors are diced into individual sensors, and the sensors are individually mounted into packages of the type used for integrated circuits, such as sealed leadless ceramic chip carriers. The packaged sensor is then mounted on a printed circuit board along with an associated control circuit, usually an IC itself and packaged in a similar manner. The sensor and control circuit, along with other circuit components as required, collectively perform the desired sensing function.

One of the drawbacks of the above-described method of packaging sensor-based systems is that individual unprotected sensors must be handled during packaging operations, potentially reducing yield and increasing manufacturing costs. Also, the sensor package is generally significantly larger and more expensive than the sensor, so the package contributes notably to the dimensions and cost of the assembled printed circuit board. Also, mounting the sensor in a package such as a chip carrier limits how close the sensor can be placed to the control integrated circuit, which in turn can unnecessarily limit the electrical performance of the sensor-based system or increase the susceptibility to noise.

It would be desirable to improve the cost, size, and performance of systems employing micromechanical sensors and associated control circuitry.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, a method of fabricating and packaging micromechanical sensors and their associated control circuitry is disclosed that eliminates the need for a separate carrier package for the sensor. The disclosed packaging method advantageously eliminates the handling of exposed sensors during packaging operations, and results in closer placement of the sensor and its associated control circuit, so that costs are reduced and greater system performance can be achieved.

In the disclosed fabrication method, a micromechanical sensor is fabricated on a semiconductor wafer, and a control circuit is fabricated on another semiconductor wafer. A cavity is etched on the back side of the control circuit wafer, the cavity being formed such that the raised portion of a sensor fabricated on the other wafer fits within the cavity when the wafers are brought together in an adjoining relationship. Through-holes are etched through the back side of the control circuit wafer to allow access to electrical contact points of the sensor circuit, and a patterned layer of metal is deposited to form electrical interconnections between the electrical contact points and termination points on the back side of the control circuit wafer via the through-holes. The termination points are arranged such that electrical contacts of the sensor contact the termination points when the wafers are placed in the adjoining relationship. The wafers are then cleaned and bonded together in the adjoining relationship. In a typical process the respective wafers contain multiple sensors and control circuits, respectively, and thus the bonded wafers are diced to yield individual bonded sensor-circuit pairs. The bonded pairs are then packaged in a known manner.

The fabrication method eliminates the need for

separate packages for the sensor and control circuit. Also, processing is done at the wafer clean room level so that the handling of individual exposed sensors is eliminated. The sensor and control circuit in each bonded pair are placed in intimate contact, thus reducing overall size and improving electrical performance, and the pairs can be packaged using conventional integrated-circuit packaging technology.

Other aspects, features, and advantages of the present invention are disclosed in the detailed description which follows.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

Figure 1 is a flow diagram of a sensor packaging method according to the present invention;

Figures 2 through 5 are schematic depictions of a control-circuit wafer at various stages in the packaging method of Figure 1; and

Figure 6 is a schematic depiction of a bonded sensor and control circuit pair resulting from the packaging method of Figure 1.

DETAILED DESCRIPTION OF THE INVENTION

In the process of Figure 1, an array of control circuits are fabricated on a semiconductor wafer at step 10 using conventional integrated-circuit fabrication techniques. The resulting control circuits may be completely custom-designed, or may be of the type known as "application-specific integrated circuits" or ASICs. The layout of the array of control circuits mirrors that of a corresponding array of sensors on a separate wafer, so that when the wafers are placed in an aligned adjoining relationship each control circuit is aligned with a corresponding sensor. This arrangement facilitates a subsequent fabrication step in which the wafers are bonded together, as described below.

Figure 2 shows a site on a wafer 30 where a single control circuit 32 is formed. Figures 2 through 6 show the results of steps from the process of Figure 1 at the site for a single sensor and control circuit pair. However, it is to be understood that the same results are obtained for each sensor and control circuit pair from the two wafers being processed, so that a complete picture of the process results would simply show an array of identical sites on the wafers.

In step 12 of Figure 1, the upper portions of the control circuit wafer 30 are removed by known mechanical and/or chemical means, resulting in a thinned wafer 30 as shown in Figure 3

In step 14, through-hole vias 34 are etched in the backside of the control circuit wafer 30 to allow access to sensor interconnection points or metallizations 33 from the backside of the control circuit wafer 30. In step 16, a second etch process is conducted to form cavities 36 for the sensors on the backside of the control circuit wafer. The results of these etching steps are shown in Figure 4.

In step 18, the back side of the control circuit wafer 30 is metallized with a patterned layer 38 of metal to create electrical interconnections in the previously-etched vias to electrical input and output points of the control circuit. The interconnections extend to include contact pads on the back side of the control circuit wafer as a part of layer 38. Corresponding contact points 39 on the sensors for input and/or output signals (I/O) are pressed against the contact pads during subsequent bonding of the wafers to complete the electrical interconnection between them. The result of the metallization step 18 is shown in Figure 5.

In step 20, the control circuit wafer 30 and a sensor wafer 40 are cleaned under high vacuum conditions. While this high vacuum is maintained, the wafers are

bonded together in step 22 using heat and/or pressure in known bonding techniques. The result of the bonding is a bonded component as shown in Figure 6 including a control circuit 32 and an associated sensor 42 interconnected with the control circuit via pads in layers 38 that contact the sensor contacts 39 and disposed in the etched cavity 36 on the back side thereof.

In the remaining steps 24 and 26, the bonded wafers are diced and the individual bonded components are packaged in an integrated circuit package such as a leadless chip carrier. The packaged component can then be mounted on a printed circuit board or other circuit substrate that provides power inputs and receives instrument outputs as required by the system in which it is used.

While the above description is of a preferred embodiment and best mode, the sensor circuit and control circuit can be placed both on outer wafer surfaces, or the control circuit placed in a back side cavity of the sensor wafer.

A method of fabricating and packaging micromechanical sensors and their associated control circuits has been shown. It will be apparent to those skilled in the art that modification to and variation of the above-described methods and apparatus are possible without departing from the inventive concepts disclosed herein. Accordingly, the invention should be viewed as limited solely by the scope and spirit of the appended claims.

CLAIMS

What is claimed is:

1. A method of packaging a micromechanical sensor with an associated control circuit, comprising:

fabricating the sensor on a front side of a first wafer of semiconductor material, said sensor having ele trical contact points of electrical I/O;

fabricating the control circuit on a front side of a second wafer of semiconductor material, said control circuit having electrical contacts;

forming a cavity on the back side of the second wafer, the cavity being formed such that the sensor fits within the cavity when the front side of the first wafer is placed in an adjoining relationship with the back side of the second wafer;

forming through-holes in the second wafer at locations adjacent to the cavity allowing access to the electrical contacts of the control circuit from the back side of the second wafer;

depositing a patterned layer of metal on the back side of the second wafer to form electrical interconnections to the electrical contacts of the control circuit via the through-holes, the interconnections terminating in back-side termination points arranged such that electrical contact points of the sensor contact the termination points when the wafers are placed in an adjoining relationship; and

bonding the first wafer and the metallized second wafer together in the adjoining relationship.

2. A method according to claim 1, further comprising the step of removing substrate material from the back side of the second wafer to reduce the thickness thereof.

3. A method according to claim 1, further comprising the step of cleaning the wafers prior to the bonding step.

4. A method according to claim 1, wherein the bonding step results in the wafers being bonded at least in an area adjacent to the sensor and control circuit, and further comprising the step of separating the bonded control circuit and sensor from the remainder of the bonded wafers.

5. A method according to claim 4, further comprising the step of packaging the bonded control circuit and sensor in an integrated-circuit package.

6. A method according to claim 5, wherein the integrated-circuit package is a leadless chip carrier.

7. A method according to claim 1, wherein the step of forming the cavity comprises etching the cavity.

8. A method according to claim 1, wherein the step of forming the through-holes comprises etching the through-holes.

9. A method of packaging micromechanical sensors and associated control circuits, comprising:

fabricating the sensors on a front side of a first wafer of semiconductor material;

fabricating the control circuits on a front side of a second wafer of semiconductor material, the control circuits being arranged such that each control circuit is mutually aligned with an associated sensor when the front side of the first wafer is placed in an adjoining relationship with the back side of the second wafer;

forming cavities on the back side of the second wafer, the cavities being arranged such that each sensor

on the first wafer fits within an associated cavity when the first and second wafers are placed in the adjoining relationship;

forming through-holes in the second wafer at locations adjacent to the cavities allowing access to electrical contact points on the front side of the second wafer from the back side thereof;

depositing a patterned layer of metal on the back side of the second wafer to form electrical interconnections between termination points on the back side of the wafer and the electrical contact points on the front side of the wafer via the through-holes, the termination points being arranged such that the electrical contacts on the front side of the first wafer contact the termination points when the wafers are placed in the adjoining relationship;

bonding the first and second wafers together in the adjoining relationship, the wafers being bonded together at least at points adjacent to the control circuits and sensors; and

cutting the bonded wafers into sections each including a control circuit and the associated sensor bonded thereto.

10. A method according to claim 9, further comprising the step of removing substrate material from the back side of the second wafer to reduce the thickness thereof.

11. A method according to claim 9, further comprising the step of cleaning the wafers prior to the bonding step.

12. A method according to claim 9, further comprising the step of packaging each bonded control circuit and sensor in a corresponding integrated-circuit package.

13. A method according to claim 12, wherein the integrated-circuit package is a leadless chip carrier.

14. A method according to claim 9, wherein the step of forming the cavities comprises etching the cavities.

15. A method according to claim 9, wherein the step of forming the through-holes comprises etching the through-holes.

16. A sensor and control circuit assembly, comprising:

a planar monolithic circuit substrate having a control circuit formed on a front side being generally aligned with the control circuit; and

a planar sensor substrate bonded to the circuit substrate, the sensor substrate having a micromechanical sensor formed thereon, the sensor being electrically connected to the control circuit via contact pads on the sensor substrate contacting the contact pads on the circuit substrate;

one said substrate having electrical interconnections between electrical connection points of one of the control circuit and sensor and contact pads on a backside of the one said substrate.

17. The assembly of claim 16 wherein a cavity if formed in a surface of one said substrate to accommodate one of said sensor and circuit.

18. The assembly of claim 17 wherein said cavity is in a back side of said circuit substrate.

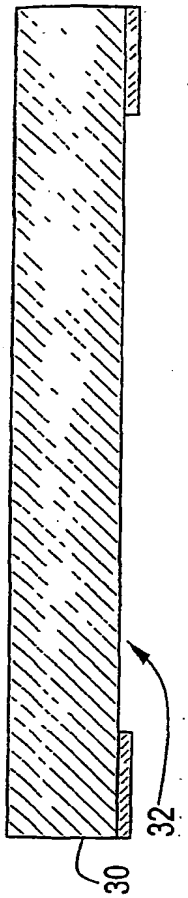


FIG. 2

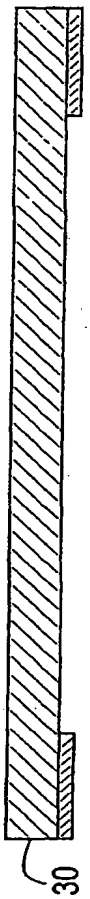


FIG. 3

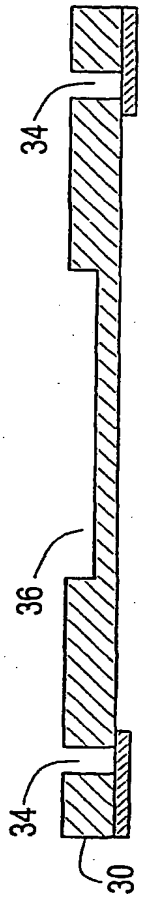


FIG. 4

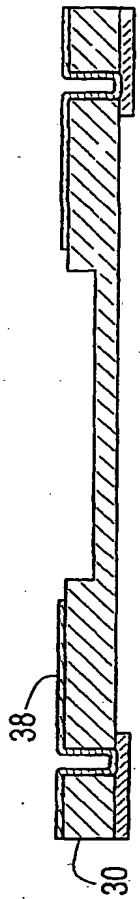


FIG. 5

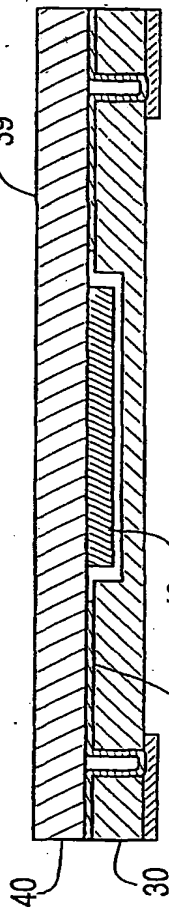


FIG. 6

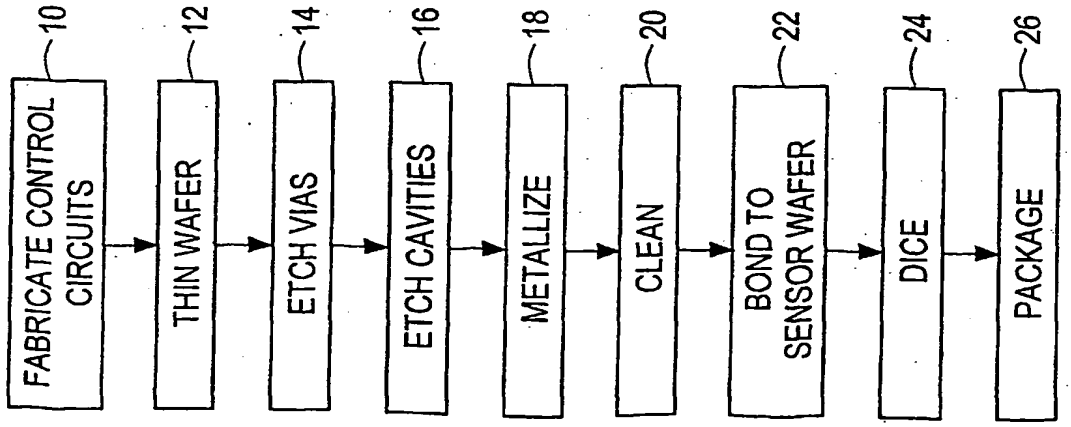


FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/41193

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 21/302, 21/48, 21/52, 21/60, 21/70; H01L 29/84, 23/02
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/48, 50, 51, 52-53, 106, 107, 110, 113, 455, 456, 458-462, 700-702, 719, 753, 977; 257/414, 417, 419; 73/861.47

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WEST, JPO, EPO, CA, INSPEC, NPL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,837,562 A (CHO) 17 November 1998 (17.11.1998), fig.5 and col-4-5.	1-18
Y, P	US 6,114,221 A (TONTI et al.) 05 September 2000 (05.09.2000), figs. 15-16, col. 3, lines 5-60.	1-18
Y	US 5,866,469 A (HAYS) 02 February 1999 (02.02.1999), fig.3B col. 3-col.4.	1-18
Y	US 5,492,596 A (CHO) 20 February 1996 (20.02.1996), see 3A-4B and col.3-col. 4.	1-18
Y	US 5,646,072 A (MAUDIE et al.) 08 July 1997 (08.07.1997), fig. 4 and col. 2, lines 59- col. 3, lines 62).	1-18

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)		
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search 20 MARCH 2001	Date of mailing of the international search report 19 APR 2001
Facsimile No. (703) 305-3230	Authorized officer AND Telephone No. SAVITRI MULPURI (703) 305-5184

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y ----- X	US 5,721,162 A (SCHUBERT et al.) 24 February 1998 (24.02.1998), detailed description.	1-15 -------- 16-18
Y ----- X	US 5,895,233 A (HIGASHI et al.) 20 Aptil 1999 (20.04.1999), detailed description.	1-15 -------- 16-18
Y, P	US 6,143,583 A (HAYS) 07 November 2000 (07.11.2000), see detailed descrption.	1-18
Y, P	US 6,074,891 A (STALLER) 13 June 2000 (13.06.2000), detailed description.	1-18
Y	US 5,712,162 A (SCHUBERT et al.) 24 February 1998 (24.02.1998), see entire document.	1-18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/41193

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

438/48, 50, 51, 52-53, 106, 107, 110, 113, 455, 456, 458-462, 700-702, 719, 753, 977; 257/414, 417, 419; 73/861.47